REPRODUCIBILITY OF ELECTROMIGRATION MEASUREMENTS

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ABSTRACT

The reproducibility of median-time-to-failure (t_{50}) measurements was determined in an interlaboratory experiment in which 11 laboratories took part with a reference laboratory. Each laboratory used a method of its choosing to test equivalent samples under the same conditions of current density and oven temperature. The between-laboratory reproducibility of t_{50} measurements normalized to one metallization temperature was dependent on current-density stress: at 1.0 MA/cm^2 it was within 15%, while at 2.5 MA/cm^2 it was generally within 50%. The primary source for variability is in estimating the temperature rise of the test metallization due to joule heating. Recommendations are given for the design and test of electromigration test structures to improve the reproducibility of t_{50} measurements.

INTRODUCTION

Electromigration is a metallization failure mechanism that is of increasing concern for the reliability assessment of VLSI-sized microelectronic devices. One aspect of this concern is the ambiguities in the electromigration characterization of metallizations due to the different test structures and measurement methods used and due to the incomplete reporting of the results from such characterizations.

To reduce the ambiguities of electromigration characterizations, an interlaboratory experiment was conducted. The purposes of this experiment were to determine the reproducibil-

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ity of characterization measurements, to identify the sources for any variability, and to develop recommendations for test structure design and for measurement procedures that improve the reproducibility of such measurements. Eleven laboratories participated with the National Bureau of Standards in this experiment.

The traditional method used to characterize the resistance of a metallization to electromigration-induced failure involves an accelerated stress test where a number of resistor test-line structures are subjected to a high current density and a high ambient temperature until they fail due to an open circuit in the test line. The median-time-to-fail, t_{50}, and the standard deviation of t_{50}, or sigma*, are the two parameters used in an electromigration characterization for a given stress condition.

EXPERIMENTAL DESIGN

All laboratories were supplied with the same type of test structures having a well-characterized metallization from one metallization lot. Each laboratory was instructed to: (1) make t_{50} measurements under two specified sets of current-density and oven-temperature stress conditions and (2) normalize the t_{50} values obtained to a common metallization temperature using a specified activation energy. The laboratories were to use procedures of their own choosing at each of these two steps.

The statistical approach for determining the reproducibility of t_{50} measurements involved the comparison of the values for the normalized median-time-to-failure, t_{50n}, reported by the participating laboratories with those obtained by a reference laboratory. The National Bureau of Standards served as the reference laboratory; it also performed the required metallization characterization measurements, measured the metallization activation energy, and determined the within-laboratory repeatability to be used in assessing between-laboratory agreement of the t_{50n} measurements.

Each laboratory was requested to provide a description of its test method and of the calculations used to obtain the t_{50n} and sigma values. A value for the metallization thickness was provided to each laboratory for determining the cross-sectional area of the test lines. The value provided was based on profilometer measurements made at five selected locations on the wafer by the reference laboratory. Each laboratory was allowed to determine

* Sigma $= \ln t_{84}/t_{50} = \ln t_{50}/t_{16}$, where the subscripts indicate the cumulative percent failure of a normal distribution.

linewidths by a method of its choice. A cross-bridge test structure on each test chip and a suggested measurement procedure were provided to allow the laboratory to make an electrical linewidth measurement [1].

Unpassivated Al 1%Si metallization was used in the experiment to permit the stress measurements to be made in a conveniently short time. The test and stress conditions specified for the experiment are listed in Table 1. All t_{50} values were to be normalized to a metallization temperature of $175°C$.

The design of the test structure and the test method used by this laboratory in the experiment are based on the results of previous work [2-4] where procedures for estimating the cross-sectional area, the temperature coefficient of resistance, and the mean stress temperature of the metallization were developed. A summary of the test method used is given in the Appendix.

TEST VEHICLE

Three test chips (2.3 by 1.7 mm) were designed for the experiment. Each chip included five straight-line resistor test structures for performing electromigration stress tests to characterize the metallization. The designed width of the test lines in these structures is three microns. The lengths of the test lines for the three chips are 400, 800, and 1200 microns. Cross-bridge test structures are located on the periphery of each chip for making measurements of the metallization sheet resistance and linewidth.

The electromigration test structures were designed to permit Kelvin-type resistance measurements to be made. The structure with the 400-micron-long test-line is shown in Fig. 1. The width of the end segments of these structures was designed to be twice the width of the test line. The fabrication process for the test structures is summarized in Table 2.

Test samples were made available to participating laboratories in three forms: (1) chips mounted in unsealed 40-pin dual-in-line ceramic packages where a thin ceramic lid, held in place with Teflon tape, was used to protect the chip; (2) chips for the laboratory to mount in its own packages; and (3) a portion of a wafer to make measurements at the wafer level. All the test samples which a laboratory received originated from the same wafer.

CHARACTERIZATION RESULTS

The test-structure resistance and the metallization sheet resistance and linewidth were measured with an automatic wafer prober and computer-controlled test system. The thickness of the metallization and of the underlying oxide insulator of each wafer were determined from profilometer and spectroscopic reflectometer measurements, respectively, made at five locations on the wafer.

The results of these measurements show that the uniformity of these parameters within a chip is better than 1% and better than approximately 3% over any wafer in the metallization lot. Linewidth uniformity over all the wafers in the lot degrades to almost 7% and accounts for an equally large variation in resistance of the test structures. The results are shown in Table 3; the value for the resistance is that for the 400-micron-long test structure. The coefficient of variation* of a parameter is the measure used to define uniformity.

Measurements of the activation energy, Q, of the metallization show that there is no discernible dependence of Q on the current density from 1.0 to 2.5 $M\dagger A/cm^2$ (contrary to an earlier prediction for such a dependence [5]) and that the mean value of Q is 0.50 eV. Test samples from one wafer were used to make the determination of Q at each current density. The test samples were stressed to failure at two oven temperatures and t_{50} values were obtained and normalized to metallization temperatures T_1 and T_2. The test conditions and measurement results are given in Table 4. Thirty-five or more test structures were used to determine each t_{50} value in the manner described in the appendix.

The within-laboratory repeatability of t_{50n} measurements was determined to be better than 8%. To make this determination, three replicate t_{50n} measurements at a current-density stress of 2.5 MA/cm^2 were made using structures with each of the three different test-line lengths. The results of the t_{50} determinations, normalized to a metallization temperature of $175°C$, and the corresponding sigma values are shown in Table 5. The estimate for the repeatability was determined from the square root of the sum of the squares of the percent coefficients of variation for the three t_{50n} means.

The results of the t_{50n} measurements listed in Table 5 also show that t_{50n} decreases with increasing line length until a length of approximately 800 microns. This is illustrated in

* Ratio of the standard deviation to the mean.

† M = mega.

Fig. 2. Such a dependence was reported earlier [6],[7] but for much shorter lines. This dependence on longer lines is attributed to the lower defect density of the metallization in these lines [8].

Because of the dependence of t_{50n} on line length, a standard test-line length is required for reproducible electromigration characterizations. The use of electromigration structures with very long test lines [9-11] has been proposed. Such structures are intended to function also as a detector of random-defects. Increasing the length of the test line, however, increases the resistance of the structure to where an excessive voltage will be generated at the desired current-density stress; it also greatly increases the area required on the chip for the structure. The use of a standard test-line length of 800 microns is recommended because its length avoids problems with short lines [2] without introducing a problem because of its resistance.

Table 5 also shows that the prediction that sigma should be a function of line length [9] is not supported by the data.

No significant wafer-to-wafer difference in t_{50n} was observed. When the t_{50n} values obtained by the reference laboratory were normalized to a mean cross-sectional area [7],[12] for the test line, the interwafer variability for both current-density stresses was approximately 8%; this is the same as the value determined for the within-laboratory repeatability of t_{50n} measurements.

INTERLABORATORY RESULTS

The results of t_{50n} and sigma determinations at a current density of 1.0 MA/cm^2 are summarized in Table 6. The normalized t_{50} values determined by the participating laboratories, t_{50n}(LAB), are listed with those determined by the reference laboratory, t_{50n}(REF). All laboratories used an equation of the form given by eq. A1 to normalize t_{50}. The ratio, t_{50n}(LAB)/t_{50n}(REF), listed for each laboratory is the measure used to assess t_{50n} data agreement, or the between-laboratory reproducibility of t_{50n} measurements.

The degree of agreement of the t_{50n} values is illustrated in Fig. 3 where the t_{50n} ratio is plotted versus a code for the participating laboratory. Exact agreement would place points on the solid line at 1.0. Agreement within the precision of the measurement by the reference laboratory is represented by the two dashed lines. These bounds represent the 8% within-laboratory repeatability that was previously determined. The between-

laboratory agreement of t_{50n} measurements is estimated to be 15% at a current density of 1.0 MA/cm^2.

The joule heating increased significantly as the current-density stress was increased from 1.0 to 2.5 MA/cm^2. The reference laboratory observed that at the lower current density the temperature rise in the metallization was generally between 4 and 5°C. The temperature rise was generally between 26 and 32°C at the higher stress, depending on the resistance of the test structures and the thermal resistance of the heat path through the package from the chip to the oven environment.

The degree of agreement of the t_{50n} values at the higher current density of 2.5 MA/cm^2 is illustrated in Fig. 4, while the t_{50n} and sigma values determined by the laboratories are listed in Table 7. The between-laboratory agreement of t_{50n} measurements at this higher current density is generally within 50%.

Test results at both levels of current density indicate that t_{50n} determinations are not affected by whether the test samples are packaged or not and if the structures on a test chip are stressed sequentially or simultaneously; this is provided that appropriate procedures are used to estimate the metallization temperature. This appears to offer the opportunity for flexibility in the manner in which electromigration structures can be tested.

ESTIMATING THE METALLIZATION TEMPERATURE

Most of the variation in the t_{50n} data resulted from underestimates of the temperature of the metallization during the stress test. Such underestimates resulted in reduced values for t_{50n} and in correspondingly lower values for the t_{50n} ratio. The effect of such underestimates on the data shown in Fig. 3 is smaller than in Fig. 4 because of the smaller amount of joule heating at the lower current-density stress.

Procedures used by laboratories led to an underestimate of the temperature of the metallization during the stress test in the following three ways:

(1) The effects of joule heating were entirely neglected. Laboratories C/D*, S, and W neglected these effects, and hence their data are the lowest in Figs. 3 and 4. The data for laboratory C/D are higher than those for the other two laboratories because it

* Laboratory C/D made t_{50n} determinations only for the higher current-density stress of packaged samples (code C) and of structures on a portion of a wafer (code D).

attempted to make a correction to the current density which served to raise the t_{50n} ratios.

(2) The temperature of the metallization due to joule heating was measured before thermal equilibrium of the chip had been established. Reports from laboratories B, G, and O indicated that this had been done. None of the other laboratories reported that this source for error had been considered.

(3) The temperature-induced increase in test-structure resistance was measured by using the structure as a two-terminal device. This had been done by laboratories A, G, and O.

Another source for the variation in data is the uncertainty in the ambient stress temperature. None of the participating laboratories indicated that package temperature measurements had been made. For the samples stressed in an oven, either the temperature of the oven interior was measured with a thermocouple inside the oven or the temperature was determined from the dial reading on the oven temperature controller. The reference laboratory measured differences of as much as $3°C$ for different packages placed in the same oven. Such differences are significant at current-density levels where the effect of joule heating is ignored and only an oven temperature measurement is made to estimate the metallization stress temperature.

The temperature of the metallization can be overestimated when all the test structures on a chip are stressed simultaneously. As each structure fails, the total power dissipation on the chip decreases and introduces an approximately step-wise decrease in chip temperature. If this is ignored, the mean temperature of the metallization of all but the first structure to fail will be overestimated.

Two adjustments in arriving at an estimate of the mean metallization temperature were not made by the participating laboratories, which led to a systematic underestimate of their t_{50n} values by approximately 5% at the higher current-density stress. One adjustment accounts for the increase in power dissipation in a test structure because of its gradual increase in resistance with stress time [3]; the other, for the voltage taps of the structure including cooler segments not part of the test line [2].

RECOMMENDATIONS

The following recommendations are made for the design and test of single-metal electromigration test structures with straight test lines. They are intended to identify key sources for measurement error in making t_{50n} determinations as identified in this interlaboratory experiment and in a related work [2].

Test Structure Design:

- o Use four-terminal, Kelvin-type structures to reduce measurement interferences.
- o Use a structure similar to the one indicated in Fig. 5, with the following design dimensions:

  Test Line: width = w, length = 800 μm.

  End-Contact Segment: width $(W) = 2w$, length $(L) > 100$ μm.

  Voltage Tap: width $(w_t) = w$, length $(T) > 100$ μm, position $(Lt) = 2W$.

- o Include a cross-bridge test structure [1] on the chip with the electromigration test structures to measure the metallization sheet resistance and linewidth.

Test Procedure:

- o Measure the metallization thickness on the originating wafer.
- o Determine the cross-sectional areas of the test lines to be stressed on a chip from an electrical measurement of the linewidth with an adjacent cross-bridge test structure.
- o Control the stress current through each test structure to within approximately 1%.
- o Use a temperature sensor in the package heat sink to monitor the temperature of each test package.
- o Determine the mean thermal response time for the metallization on the test chip to attain an equilibrium temperature after a step-wise increase in power dissipation on the chip.
- o Determine a mean value for the temperature coefficients of resistance (TCR) of the

test structures.

- o Determine, from the increase in test structure resistance and the mean TCR, the temperature of each test structure, $T(TS)_p$, approximately one thermal response time after the initiation of the stress test.

- o Determine the mean temperature of the test structure during its stress test by subtracting the temperature of the heat sink, $T(HS)_p$, at the time that $T(TS)_p$ was measured, from the sum of $T(TS)_p$ and the mean temperature of the package heat sink, averaged over the life of the structure in the test.

- o Monitor each test structure for failure at intervals that are short compared to the expected value for t_{50}.

- o Calculate t_{fn}, the time-to-fail of each structure, normalized to the metallization temperature T_n, by using eq. A1.

- o Determine the normalized t_{50} for the structures stressed to failure from a linear regression analysis of the $\ln(t_{fn})$ data versus the normal cumulative percent failure distribution. Calculate the cumulative percent failure in units of 1/(N+1), where N is the number of structures stressed.

SUMMARY

An interlaboratory experiment was conducted involving nine commercial laboratories, two university laboratories, and a reference laboratory. The participating laboratories were provided with equivalent test samples to make electromigration median-time-to-failure determinations by a method of its choosing under two sets of current-density and oven-temperature conditions. The laboratories were also provided with a value for the metallization thickness for use in determining the stress currents, and with an activation energy for use in normalizing their t_{50} data to a metallization temperature of $175°C$.

The between-laboratory reproducibility of t_{50n} determinations was found to be dependent on the degree of joule heating in the metallization. At a current density of 1.0 MA/cm^2, where the joule heating is small, the reproducibility is within approximately 15%. The reproducibility is more variable but generally within 50% at a current density of 2.5 MA/cm^2. The primary source for variability of t_{50n} determinations is in estimating the temperature rise of the metallization due to the joule heating in the test structure.

The within-laboratory repeatability of t_{50n} measurements by the reference laboratory was better than 8% at a current-density stress of 2.5 MA/cm^2. A dependence of t_{50n} on line length was observed for lengths less than approximately 800 microns. No dependence of sigma on test line length was observed. No dependence of the activation energy on current-density stress was observed.

Recommendations are given for the design and test of electromigration test structures to improve the reproducibility of t_{50n} measurements. The procedure used by the reference laboratory is given in the Appendix.

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APPENDIX: TEST PROCEDURE USED BY THE REFERENCE LABORATORY

The sockets used to hold and make electrical contact to the test packages featured a slot which accommodated a 3-mm-thick copper block, 9 mm wide and 52 mm long, which was used as the heat sink for the package. A silicone heat-conducting compound was used at the interface between the package and the heat sink to promote good thermal contact. The temperature of each heat sink was measured with a thermocouple located at the end of a hole in the heat sink which extended to beneath the center of the chip.

The test structures in each test package were visually inspected to assure the absence of unwanted physical anomalies in the test lines. Electrical determinations at room temperature were made of the metallization linewidth and sheet resistance using the cross-bridge test structure on each chip. These were used to correct for possible variations in cross-sectional area of the test lines on the chip in a manner previously described [4]. The areas and the previously determined metallization thickness were used to determine the stress current through each test structure required to attain the desired current density stress in the test line.

All the structures stressed were electrically connected in parallel to a voltage source maintained at 10 V during the stress test. A variable load resistor connected in series with each structure was used to maintain the desired stress current through the test structure to within 1% for the life of the structure. The current through each structure was determined from measuring the voltage across a one-ohm resistor, also in series with the structure.

The resistance of each test structure and the temperature of each respective package heat sink were measured at room temperature.

The package heat sinks were maintained by the test ovens at a constant stress temperature, plus or minus a standard deviation of less than $0.3°C$. A nitrogen gas environment was maintained in the oven during the tests with a nitrogen flow rate of approximately 10 std. ℓ/min. The resistance of each test structure and the temperature of each respective package heat sink, $T(HS)_o$, were measured at the oven stress temperature, and the temperature coefficient of resistance was calculated for each structure.

The resistance of the structures and the package heat sinks were measured again at ap-

proximately one thermal response time after applying the stress current to determine the joule-induced temperature rise of each structure above that of its respective package, $T(TS)_p - T(HS)_p$. The previously determined thermal response time of the system was approximately 15 minutes. During the stress test, both the voltage across each structure and the temperature of the heat sinks were recorded every 15 minutes but monitored approximately every minute to detect and record the time of failure.

An estimate of the mean temperature of each test line during its life in the test was determined using the following procedure: Initially, the power dissipation in each test structure is assumed to be constant. The metallization temperature of a given structure on the chip is then given by $[T(TS)_p - T(HS)_p] + T(HS)_m$, where $T(HS)_m$ is the mean temperature of the heat sink for the life of the test structure in that package. The mean temperature of the heat sink is calculated by assuming that, as each structure fails, the temperature of the heat sink will fall by one fifth of the original temperature rise of the heat sink when the stress current was applied to all five structures on the chip; namely: $T(HS)_p - T(HS)_o$. The mean metallization is then corrected [3] by accounting for the increase in power dissipation in the test structure due to an assumed quadratic increase of its resistance with stress time.

The calculated time-to-fail, t_f, of each test structure for the estimated metallization temperature was then normalized to a metallization temperature of $175°C$ by using the relation

$$t_{fn} = t_f \exp\left[\frac{eQ}{k}(1/T_n - 1/T)\right] \qquad (A1)$$

where T and T_n are the estimated and normalized metallization temperatures, respectively, and where k is Boltzmann's constant and e is the electronic charge.

The normalized median-time-to-failure, t_{50n}, was determined from a linear regression analysis of the t_{fn} values. A final correction was made to the t_{50} value for the 400-micron-long structures with an equation of the form given by eq. A1 to account for the difference between the mean temperature of the test structure, which is what is measured by the resistance change of the structure, and the mean temperature of the test line [2],[3]. The temperature correction is approximately $0.5°C$ for these structures. For the longer structures, this correction is much smaller and was neglected.

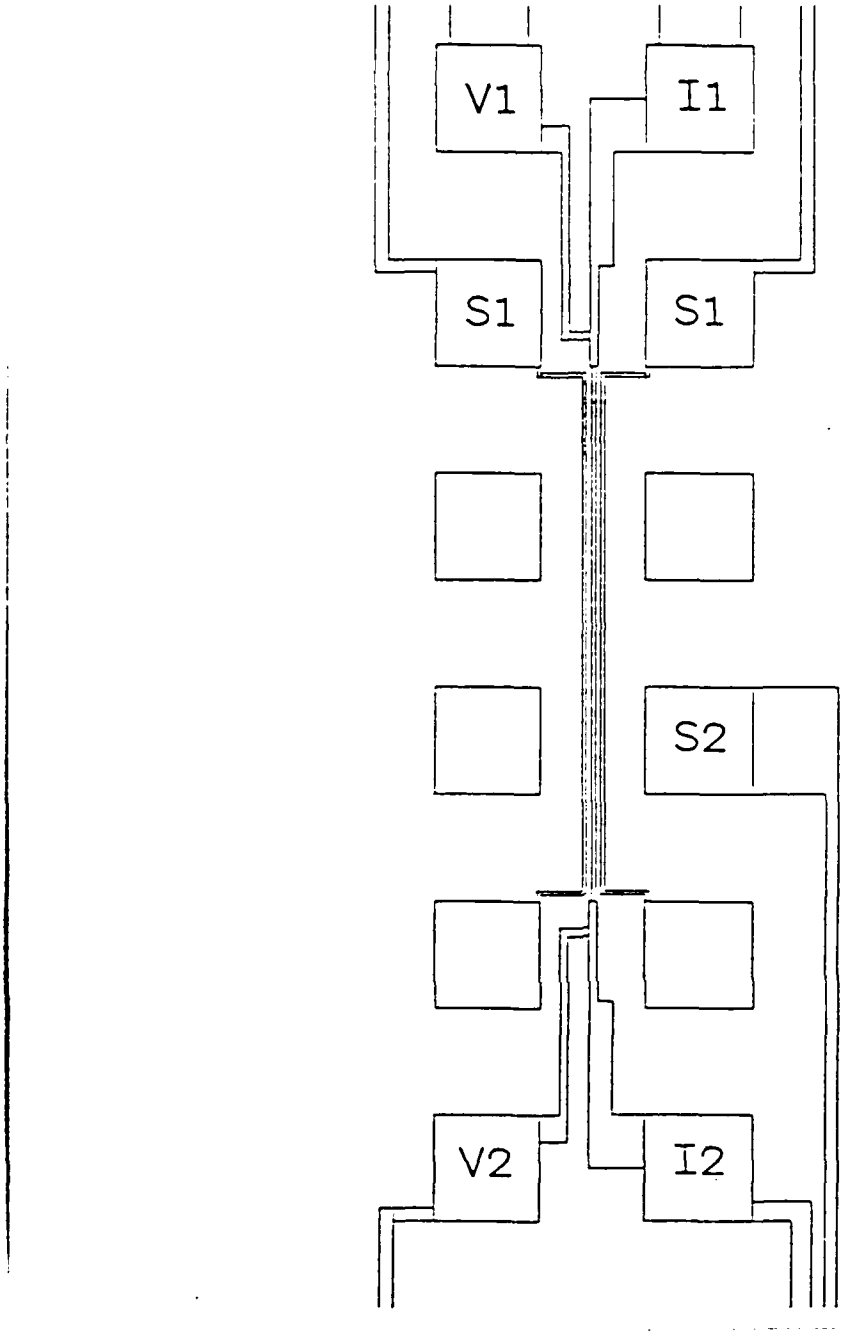

Fig. 1. An electromigration test structure whose test line is 400 microns long. Contacts S_1 and S_2 were not used in the experiment.

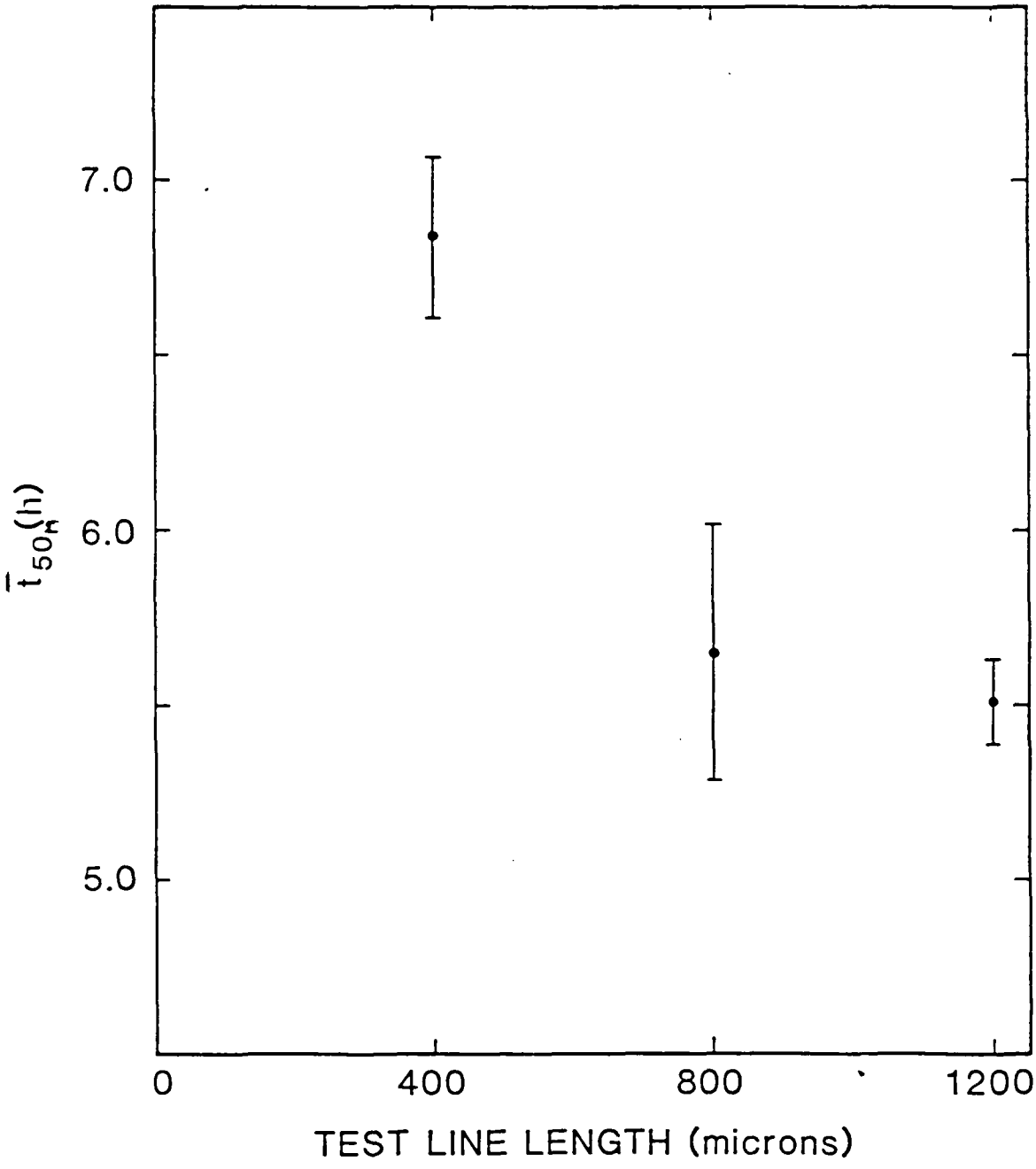

Fig. 2. Mean of three replicate measurements of t_{50n} at three test-line lengths. Error bars are the standard errors of the mean.

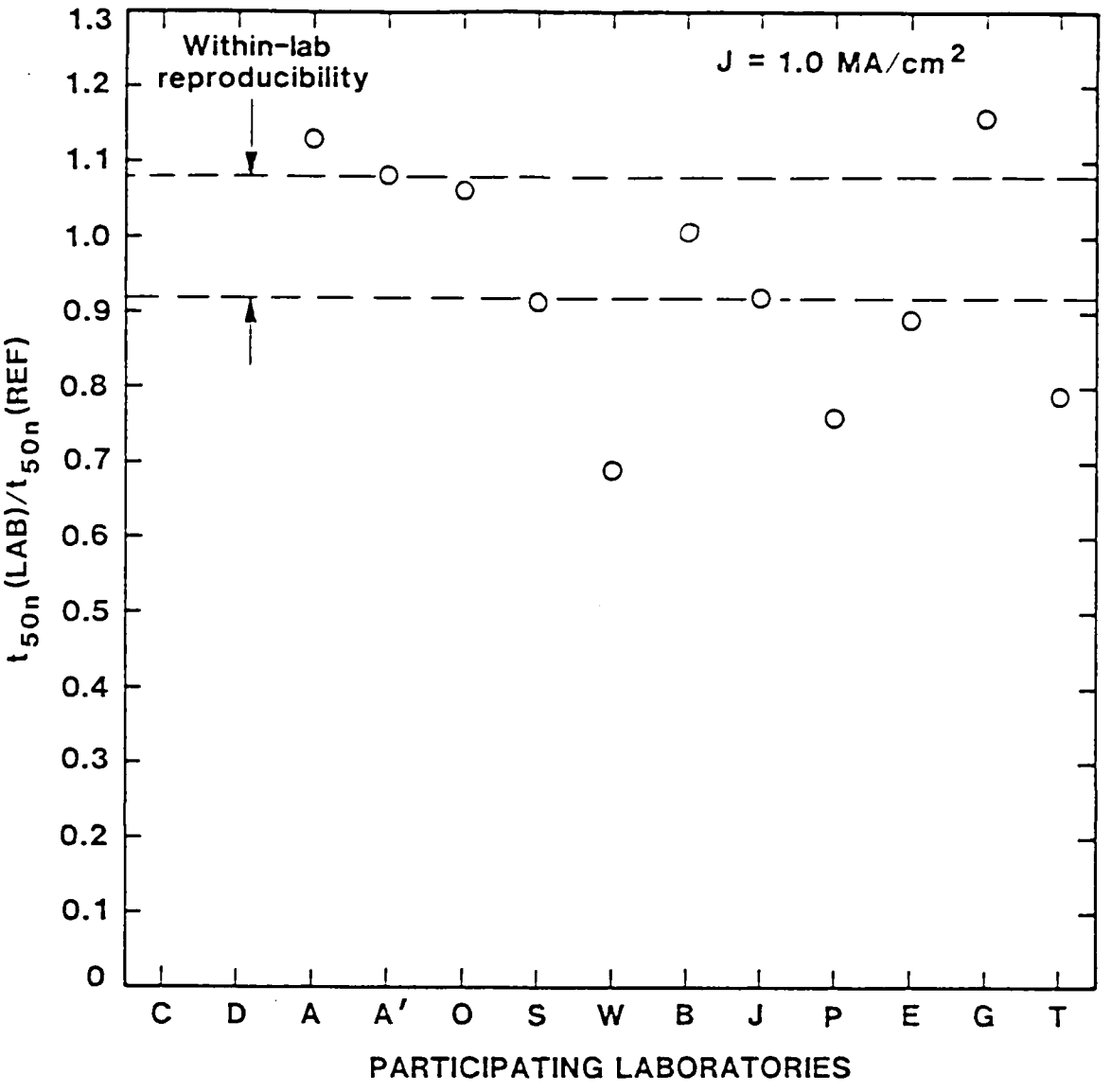

Fig. 3. Listing by participating laboratory of the ratio of the normalized t_{50} value reported by these laboratories to the value obtained by the reference laboratory when measuring parts from the same wafer as the reporting laboratory.

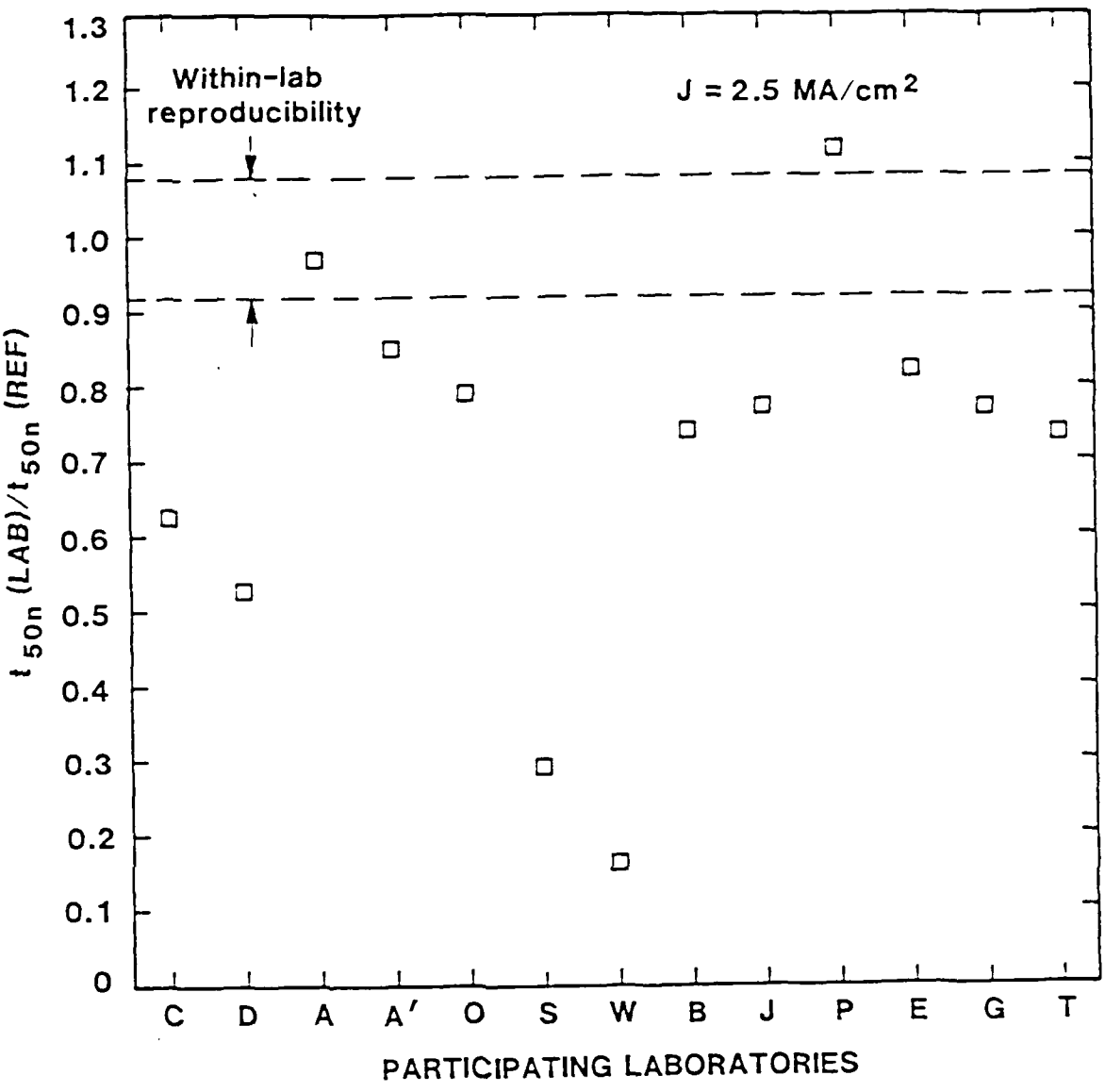

Fig. 4. Listing by participating laboratory of the ratio of the normalized t_{50} value reported by these laboratories to the value obtained by the reference laboratory when measuring parts from the same wafer as the reporting laboratory.

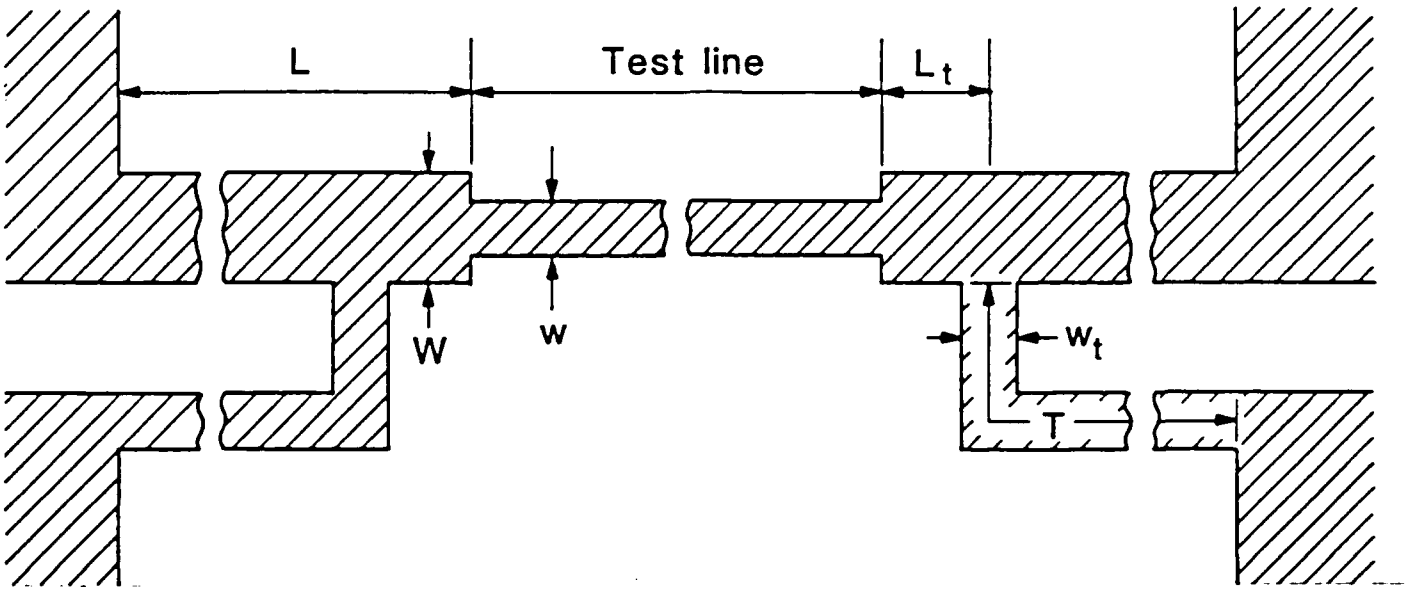

Fig. 5. Basic elements of recommended electromigration test structure.

Table 1. Test and Stress Conditions of Experiment

Number of Test Structures	Current Density (MA/cm^2)	Oven Temperature (°C)
20	1.0	175
20	2.5	150

Table 2. Test Structure Fabrication

PASSIVATION	UNDERLYING INSULATOR
none	LPCVD (8% P) SiO2, 0.6 μm thick over field SiO2, 1.0 μm thick
METALLIZATION	
alloy: Al, 1% Si deposition: sputter etch process: wet anneal process: 20 min in Forming gas at 450 deg. C	SUBSTRATE Si(100), p-type

Table 3. Parameter grand means and estimates of parameter uniformity for a lot of six test wafers.

		Parameter Uniformity Within		
Parameter	Grand Mean	Lot	Wafer	Quadrant
Resistance	5.07 ohm	7.2%	3.3%	0.9%
Sheet resistance	36.8 milliohm per square	1.2%	2.7%	0.5%
Linewidth	3.10 microns	6.9%	2.0%	0.6%
Thickness	0.86 microns	1.8%	2.7%	--
Thickness (oxide)	1.56 microns	0.6%	0.9%	--

Table 4. Measurement of activation energy at two levels of current density.

J (MA/cm^2)	T1 (deg C)	T2 (deg C)	Delta T (deg C)	Q (eV)
1.0	179	218	39	0.495
2.5	144	185	41	0.502

Table 5. Results of three replicate t_{50n} measurements of test structures with three different test-line lengths. The t_{50n} values are for a current-density stress of 2.5 MA/cm^2, normalized to a metallization temperature of 175 $°C$. Twenty test structures were used to determine each t_{50n} value.

	L=400 microns		L=800 microns		L=1200 microns	
	t_{50N}(h)	Sigma	t_{50N}(h)	Sigma	t_{50N}(h)	Sigma
	7.31	0.26	5.50	0.31	5.26	0.26
	6.68	0.24	5.10	0.26	5.64	0.24
	6.53	0.29	6.36	0.25	5.63	0.27
Sigma:		0.27		0.27		0.25
t_{50N}(h):	6.84		5.65		5.51	
SD (h):	0.41		0.64		0.22	
SD/t_{50N}:	6.0%		11.3%		4.0%	

Table 6. t_{50} and sigma values of the participating and reference laboratories for a current-density stress of 1.0 MA/cm^2, normalized to a metallization temperature of 175 °C. Laboratory codes A and A′ are for the same laboratory where two workers used different approaches to determine the metallization stress temperature.

J = 1.0 MA/cm^2

	LABORATORY		REFERENCE		$\frac{t_{50n}(LAB)}{t_{50n}(REF)}$
LAB ID	t_{50n} (h)	SIGMA	t_{50n} (h)	SIGMA	
A	40.3	0.4	35.70	0.31	1.13
A′	38.5	0.4	35.70	0.31	1.08
O	32.22	0.32	30.99	0.35	1.06
S	27.69	0.36	30.39	0.35	0.91
W	21.0	0.29	30.39	0.35	0.69
B	30.8	0.36	30.39	0.35	1.01
J	25.6	0.42	27.88	0.27	0.92
P	28.1	0.35	37.13	0.30	0.76
E	32.92	0.36	37.13	0.30	0.89
G	35.97	0.44	30.99	0.36	1.16
T	28.10	0.25	35.85	0.37	0.78

Table 7. t_{50} and sigma values of the participating and reference laboratories for a current-density stress of 2.5 MA/cm^2, normalized to a metallization temperature of 175 °C.

J = 2.5 MA/cm^2

	LABORATORY		REFERENCE		$\frac{t_{50n}(LAB)}{t_{50n}(REF)}$
LAB ID	t_{50n} (h)	SIGMA	t_{50n} (h)	SIGMA	
C	3.55	0.29	5.64	0.24	0.63
D	3.00	0.35	5.64	0.24	0.53
A	6.53	0.30	6.76	0.27	0.97
A′	5.77	0.32	6.76	0.27	0.85
O	4.44	0.34	5.65	0.25	0.79
S	1.77	0.44	6.11	0.23	0.29
W	0.97	0.45	6.11	0.23	0.16
B	4.53	0.28	6.11	0.23	0.74
J	4.32	0.41	5.64	0.24	0.77
P	6.69	0.28	6.02	0.25	1.11
E	4.95	0.30	6.02	0.25	0.82
G	4.36	0.43	5.65	0.25	0.77
T	4.49	0.40	6.17	0.35	0.73